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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/515,358	02/29/2000	Philip A Bourekas	M-7949US	1167

24251 7590 10/27/2003

SKJERVEN MORRILL LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110

EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2189	11

DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PR4

Office Action Summary	Application No.	Applicant(s)	
	09/515,358	BOUREKAS, PHILIP A	
	Examiner	Art Unit	
	Kim T. Huynh	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8,10-15 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2- 5, 8, 10-13, 17-22, 24* is/are rejected.

7)☒ Claim(s) *6,7,11,14,15 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 February 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 6-7 , 11 , 14-15, 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art fails to teach or suggest wherein a portion of set of exception registers is for servicing interrupts and another portion is for servicing operating system calls and wherein servicing exception using at least one set of exception registers modifying the values of the registers in set of exception registers without disrupting the state of the interrupted task.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 2- 5, 8, 10-13, 17-22, 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen et al. (US Patent 5,115,506)

As per claim 2, Cohen discloses a processor comprising:

- A set of general purpose registers; and ((col.2, lines 34-37), wherein normal implies general purpose registers)

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- A set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers during servicing of an exception, wherein said set of exception registers is substantially dedicated for servicing exceptions. (col.6, lines 1-11)

As per claim 3, Cohen discloses wherein said set of exception registers is for servicing exceptions having a high priority not for those exceptions having a low registers is for servicing exceptions having a high priority not for those exceptions having a low priority. (col.5, line 56-col.6, line 11), (col.2, line 50-col.3, line 7)

As per claim 4, Cohen discloses Cohen discloses wherein said processor provides a dedicated vector to said set of exception registers for said exception. (see abstract)

As per claim 5, Cohen discloses wherein there are at least eight exception registers. (col.3, lines 8-28)

As per claim 8, Cohen discloses a select logic circuit having a first input terminal that receives an exception register active bit and a second input terminal that receives a register address bit, said select logic circuit provides an output signal on an output terminal used to select between said set of general purpose registers and said exception registers. (col.3, lines 8-40), (col.4, lines 25-45)

As per claim 10, Cohen discloses wherein said at least one set exception registers is a dedicated set of exception registers. (col.3, lines 29-40), (col.4, lines 8-15)

As per claim 12, Cohen discloses a method of interrupting the execution of a task and servicing an exception in a processor, said method comprising:

- swapping a set of general purpose registers for at least one set of exception registers if an exception asserted at said processor is a high priority exception; (col.6, lines 1-11)
- servicing said exception using said at least one set of exception registers if said exception is a high priority exception; (col.5, line 56-col.6, line 11), (col.2, line 50-col.3, line 7)
- preserving information from the set of general purpose registers in a memory if said exception is a low priority exception; and (col.2, line 50-col.3, line 7)
- swapping out said exception registers for said set of general purpose registers and resuming execution of said task if said exception is a high priority exception. (col.6, lines 1-11)

As per claim 13, Cohen discloses wherein said first vector is a dedicated vector and said providing said first vector automatically separates said high priority exception from said lower priority exceptions. (col.2, line 50-col.3, line 35), (col.4, lines 8-24)

As per claim 17, Cohen discloses an apparatus for executing tasks and servicing exceptions, said apparatus comprising:

- Means for interrupting a task when an exception is asserted; (col.6, lines 1-11)

- Means for servicing said exception without disrupting the state of the interrupted task, including means for activating at least one set of dedicated exception registers; and (col.4, lines 8-24)
- Means for resuming execution of said interrupted task, including means for deactivating said dedicated exception registers and activating general purpose registers and activating general purpose registers to resume execution of said task. (col.4, line 8-col.6, line 27)

As per claim 18, Cohen discloses wherein said means for activating comprises a first select logic circuit coupled to said set of general purpose registers and a second select logic circuit coupled to said at least one set of exception registers, said second select logic circuit receives an execution register active bit enabling said at least one set of exception registers and said second select logic circuit receives an inverted execution register active bit disabling said set of general purpose registers. (col.4, line 8-col.6, line 27)

As per claim 19, Cohen discloses wherein said servicing comprises providing a first vector and activating said at least one set of exception registers for said high priority exception, and wherein said providing comprises providing a second vector and not activating said set of exception registers for lower priority exceptions. (col.4, line 8-col.6, line 27)

As per claim 20, Cohen discloses a process comprising:

- A set of general purpose registers; and((col.2, lines 34-37), wherein normal implies general purpose registers)
- A set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers only when an exception having at least a predetermined priority level is detected by said processor and that are not switched when an exception having a priority less than the predetermined priority level is detected by said processor. (col.6, lines 1-11), (col.4, lines 8-45)

As per claim 21, Cohen discloses another set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers only when another exception having at least said predetermined priority level is detected by the processor while said set if dedicated exception registers are switched for at least the subset of said set of general purpose registers. (col.6, lines 1-11), (col.4, lines 8-45)

As per claim 22, Cohen discloses the processor further comprising a select logic circuit having a first input that receives an exception register active bit and a second input that receives a register address bit, said select logic circuit provides an output signal on an output used to select between said set of general purpose registers and said exception registers. (col.3, lines 8-40), (col.4, lines 25-45)

As per claim 24, Cohen discloses wherein said set of dedicated exception registers is switched only when an exception, of a first type, having at least a predetermined priority level is detected by said processor and the

processor further comprising another set of dedicated exception registers that are switched for at least a subset of said set of general purpose registers only when another exception, of a second type, having at least said predetermined priority level is detected by the processor. (col.6, lines 1-11), (col.4, lines 8-45)

Response to Arguments

4. Applicant's arguments filed on 8/7/03 have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Daniel et al. [USPN 5,987,258] discloses register reservation method for fast context switching in microprocessors

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM-6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

Oct. 13, 2003

XUAN M. THAI
PRIMARY EXAMINER
TC 2100